Q-10

LONG TERM STABILITY OF DROs COMPARED TO CRYSTAL OSCILLATORS

*K.R. VARIAN**

Rockwell International
Dallas, Texas 75207

ABSTRACT

Guidelines are presented for GaAs FET DRO's which when followed result in the DRO's long term drift characteristics being similar to crystal oscillators. The guidelines fall into three categories: electrical stresses in the FET, fabrication issues of the DRO, and processing of the FET (a screening test for the GaAs FETs is described). Experimental data is included on a sample of units that support the proposed guidelines.

INTRODUCTION

The use of Dielectric Resonate Oscillators (DROs) has been proposed in systems since their inception. DROs are usually smaller, more efficient, more reliable, and easier to construct than their mechanical counter parts. In Digital telecommunication systems an added advantage is that DROs have less tendency to suddenly jump frequency (known as a glitch or hit in the system). With all of these pluses, DROs have yet to be used successfully in Digital telecommunication systems because of their lack of long term stability (that is existence of long term drift). This paper will present data that supports the idea that DROs can be manufactured to obtain stability comparable to crystal oscillators. The 4 GHz long term drift measurements reported in this paper are based on the DRO described in [1].

Long term drift is the varying of oscillator resonate frequency with time at a constant rate. In figure 1, several curves representing different kinds of frequency variation are presented. Curve a) is a classic example of long term drift unlike curves b) through d). Curve b) is an example of a sudden jump in frequency. Curve c) is a unit that will vary with time in a sinusoidal nature due to some component being thermally cycled. Curve d) is an example of a unit that has a short term drift but after a time the drift rate decreases to a different rate. The final two curves exhibits no signs of long term drift. Curve e) exhibits a short term drift that after a certain length of time stabilizes. The final curve in the series demonstrates a unit with no long term drift. Data on units that do exhibit long term drift is shown in Figure 2. These curves are of an 11 GHz ovenized FET DRO (oven temperature of approximately 90°C) operating at room temperature. The data was taken at weekly intervals. Ignoring the unit that jumped in frequency and data fluctuation, it is clear that all of the units exhibit a long term drift rate of .35 ppm/day.

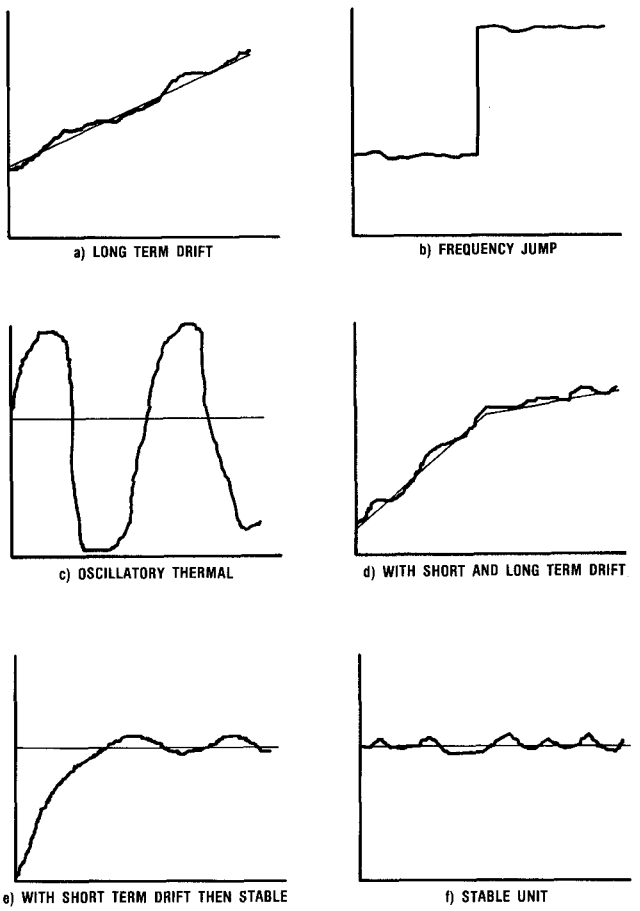

Figure 1. Variations of Frequency with Time

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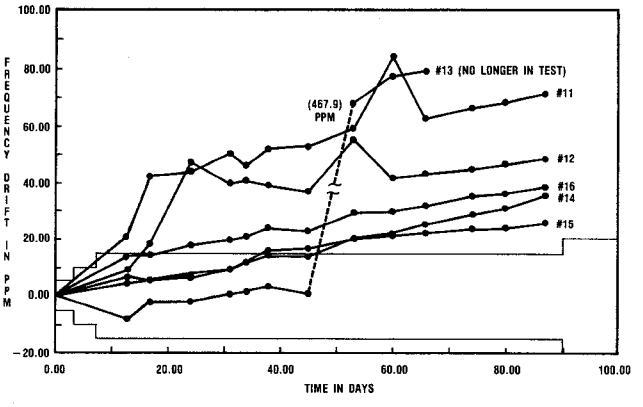


Figure 2. Units with Long Term Drift

What is an acceptable long term drift criteria for DROs? A starting point was to use the same criteria that is placed on crystal oscillators with "green" crystals. "Green" crystals are crystals that have not been subjugated to a high temperature bake after the fabrication. The high temperature bake is used to remove the mechanical stresses that are induced from the manufacturing process. The frequency adjustment criteria for crystal oscillators with "green" crystals was chosen as a starting point. To this criteria was added one additional adjustment period. The additional adjustment period for the free running DROs was at the one week interval. The frequency adjustment periods and acceptable frequency accuracies are given in Table 1. Drawing this specification on Figure 2, one can see that none of the units meet the criteria.

Time	Drift Between Settings		Total Drift From Turn-on	
	PPM	Frequency	PPM	Frequency
72 Hours	±5 PPM	±20 KHz	±5 PPM	±20 KHz
1 Week	±5 PPM	±20 KHz	±10 PPM	±40 KHz
3 Months	±5 PPM	±20 KHz	±15 PPM	±60 KHz
6 Months	±5 PPM	±20 KHz	±20 PPM	±80 KHz
9 Months	±5 PPM	±20 KHz	±25 PPM	±100 KHz
1 Year	±5 PPM	±20 KHz	±30 PPM	±120 KHz
18 Months	±5 PPM	±20 KHz	±35 PPM	±140 KHz
2 Years	±5 PPM	±20 KHz	±40 PPM	±160 KHz
Every year thereafter	±5 PPM	±20 KHz		

Table 1. Drift after turn-on for Crystal Oscillators with "Green" Crystals

The DRO is described in detail in [1] and consists of an active device, a dielectric resonator, input and output coupling lines, biasing line, blocking capacitors, terminating components, and optionally, some attenuators. After analyzing the possible candidates for the cause of long term drift, the following areas were considered; electrical stresses to the parts, thermal stresses to the parts, aging of the dielectric resonator, mechanical stresses in the assembly, the epoxy bonds in the assembly, mechanical stress caused by soldering the chip components, and aging of the active device. The following paragraphs outline the results of the investigation into each of these areas.

Stresses were not covered in [1] and are detailed in Table 2. None of the factors were stressed to greater than 50% of rated maximums except the maximum operating temperature.

	Absolute	Design	Percentage
V_{ds} (max)	20 Vdc	8.8 Vdc	44%
I_d (max)	600 ma	140 ma	23%
P_t (max)	3 W	1.23 W	41%
T_{chan} (max)	150°C	141°C	94%

Table 2. FET Stresses

Accelerated life testing was performed on the dielectric resonator. No indication of long term drift effects were detected. This is supported by vendor data.

Mechanical stresses in the assembly can traditionally be removed by thermal cycling of the unit. This was done and no significant changes in long term drift were detected.

The resonator is held in place by an epoxy. Many different epoxies were tried with no significant change in long term drift. The variations tried are epoxies with different bonding strengths and different sized molecular molecules. The essential factor observed was that the epoxy to metal, plastic, or resonator material bonds must be flawless.

Another Mechanical stress is in the attachment of chip components. It was found that the stresses introduced by bonding one end and then the other of a chip would lead to a stress that could take up to a month to be removed. To minimize this initial drift rate, all of the units were bonded with a hot air machine that permitted simultaneous bonding of both ends of the component.

The final and most likely cause of the long term drift is the active device. Since a FET was chosen as the active device the most likely candidate (that is most mechanically critical) is the gate structure. Tests to check the integrity of the gate were determined and will be described later.

RESULTS OF FOLLOWING DESIGN AND FABRICATION GUIDELINES

Figure 3 illustrates the long term drift of the prototype units. These units were not assembled using the hot air machine and this is the reason for the initial drift rate. This was confirmed on subsequent built units. Although the results are not impressive, there are several keys points to note. All of the units have an initial high drift rate. But after being operational for a length of time, all of the units stabilized. Some of the units were returned around 30 days after turn-on. This readjustment was to see the effect of retuning on long term drift. The retuning only shifted the curve. Note especially in the 90 to 150 day period (except for jarring of the setup or loss of DC power) there is not significant drift. Due to the lack of drift in the 90 to 150 day time period, efforts were focused on the initial high drift rate. Another item to note is that none of the units exhibited any frequency jumps.

Figure 4 shows the long term drift of several of the latest units built. These units incorporated the above mentioned improvements in the design and one

can see that the results are very consistent. Note especially, that the high initial drift rates are removed but there is still a slight upward, drifting tendency. The rate of the drift is approximately .08 ppm/day. This rate is better by a factor of four than the rate shown for the 11 GHz units in Figure 2.

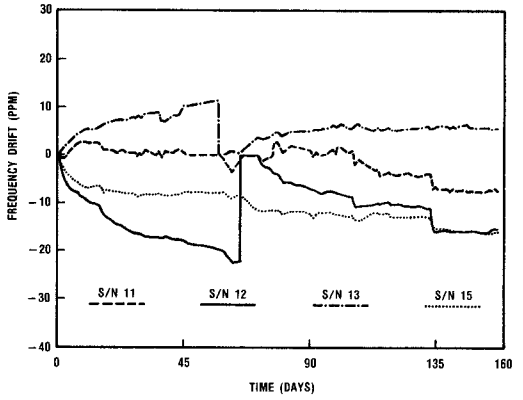


Figure 3. Long Term Drift of Prototype Units

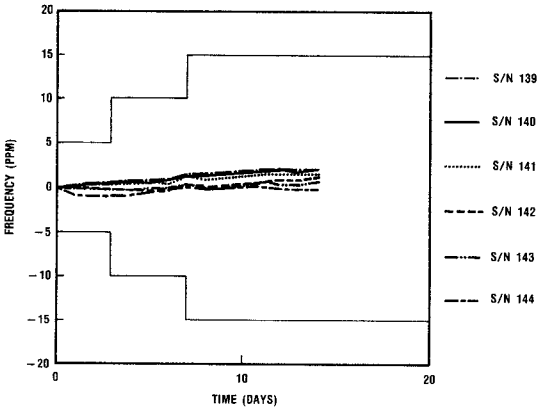


Figure 4. Long Term Drift of Recently Built Units. No screening of FET

The slight drifting tendency was further confirmed during the next build cycle when over 100 DRO's were fabricated. The units were subjected to a two week screening test to remove units with a high constant drift, a histogram of the drift rate is shown in Figure 5. The drift rate indicated on these curves is during the first to second week. Since the long term goal of the DROs is to meet a drift of less than 5 ppm/year this final drift rate was investigated.

SCREENING PROCEDURE OF FETs

As mentioned earlier, in regards to the FET, the integrity of the gate was considered the cause of long term drift of the DROs. The thought was that the gate capacitance was changing due to the surface states changing the apparent capacitance of the gate. To check as to whether or not the drift was caused by a change in surface states, it was suggested [2] to measure the gate capacitance of the FETs. To this end, the following measurements were performed.

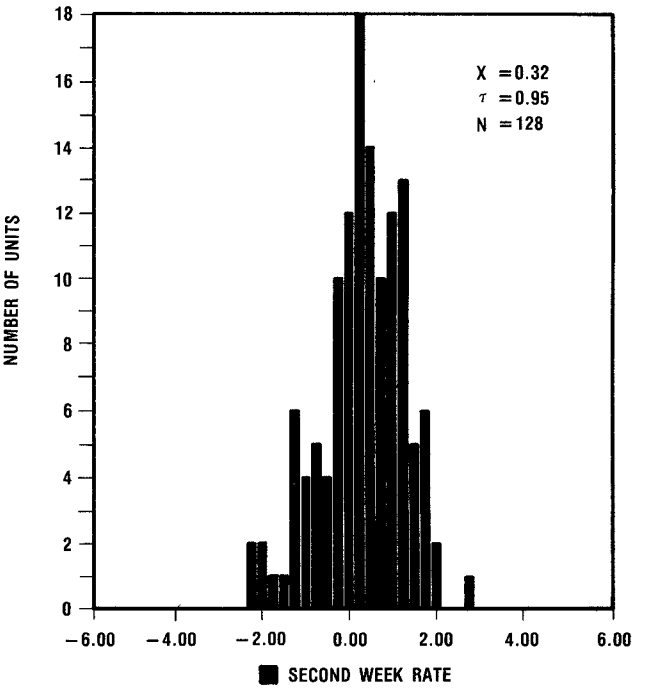


Figure 5. Long Term Drift Rate of First 128 Units. No Screening of FET

The total gate capacitance was measured on twenty-four units. The capacitance measured was the sum of the gate package capacitance and the capacitance between the gate and the source, drain, and substrate of the FET. The FETs were then placed in an oven and baked at 180°C for four hours. During the baking no electrical power was applied to the FETs. After baking, the total gate capacitance was again measured on the units.

The data was then reduced to plots of $1/C^2$ versus gate voltage [3] as shown in Figure 6. The capacitance that was used (C_g) was the capacitance at the desired gate voltage (C_{gm}) minus the capacitance at a gate voltage of -5 Vdc (C_{g5}), this is indicated by the following equation.

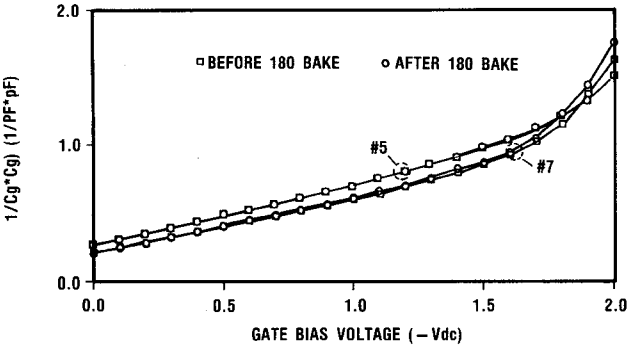
$$C_g = C_{gm} - C_{g5}$$

An examination of the data on the twenty-four units indicated that some of the units exhibited no change at all, depicted in Figure 6a, while the rest of the units did show a change, as depicted in Figure 6b.

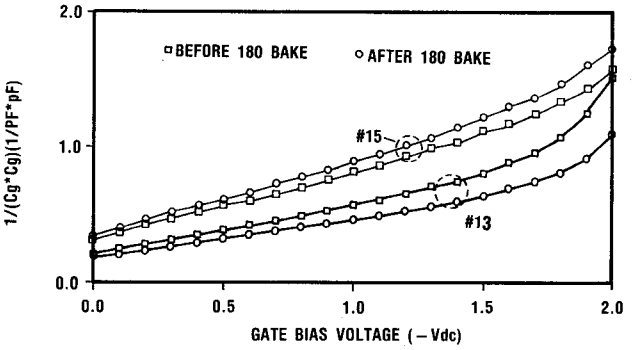
RESULTS USING THE SCREENED FETs

Long term drift tests were then initiated to determine whether the variation in capacitance was the cause of long term drift in the DROs. Ten FETs

were selected and placed into untested DROs. Five of the FETs were chosen from the units that exhibited no change in the gate capacitance, while the other five were those that changed the most.



a) Stable Capacitance



b) Non-stable Capacitance

Figure 6. Effect of Baking FETs a) No Significant Change b) Change in Gate Capacitance Due to 4 hour bake at 180 Degrees C

The results of the long term drift test is shown in Figures 7 and 8. The results are that the FETs which did not change with the 180°C bake, exhibited little long term drift. While the units that did exhibit a change in the gate capacitance when baked did exhibit long term drift.

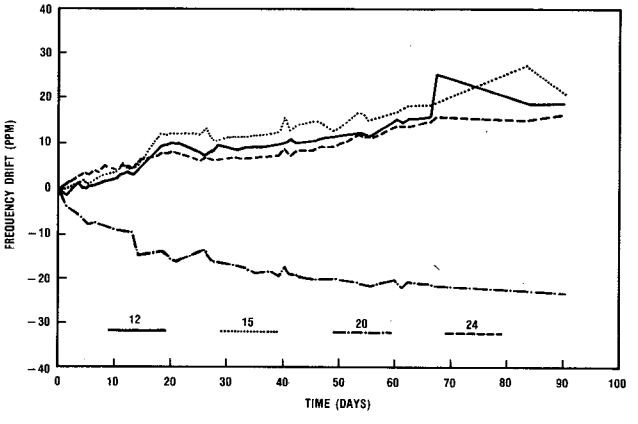


Figure 7. DROs Built with FETs that had a Significant Change in Gate Capacitance

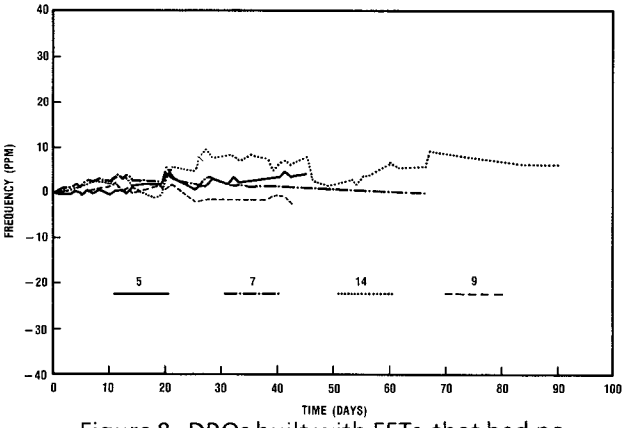


Figure 8. DROs built with FETs that had no Significant Change in Gate Capacitance

CONCLUSION

In conclusion, units can be built with long term drift stabilities approaching that of crystal oscillators if the subsequent guidelines are followed:

1. Electrical stresses to the FET must be less than 50% of the maximum rated values.
2. Keep the channel temperature of the GaAs FET to less than 150°C.
3. All epoxy bonds are flawless.
4. Minimize the electro-mechanical stresses that cause the initial high drift rate.
5. Screen the FET to minimize the change of gate capacitance with time.

REFERENCES

[1] K. R. Varian, " DRO's AT 4, 6, AND 11 GHz," IEEE-MTT Symposium, 1986.

[2] H. Kroemer, Private communication.

[3] S. M. Sze, "SEMICONDUCTOR DEVICES PHYSICS AND TECHNOLOGY," John Wiley & Sons, 1985.

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